# CLAIMS

What is claimed is:

1. A method for reading memory values, comprising:
   sampling a plurality of magnetic memory elements, wherein the memory elements contain unknown values;
   buffering the sampled values;
   writing known values to the plurality of memory elements;
   sampling the plurality of memory elements, wherein the memory elements contain known values; and
   comparing the known values to the buffered values.

2. The method of claim 1, further comprising restoring the initial unknown values to the memory elements.

3. The method of claim 2, wherein initial unknown values of memory elements are restored only if the known and unknown values do not match.

4. The method of claim 1, wherein sampling the memory element includes:
   regulating a voltage across a magnetic memory element; and
   correlating the resistance of a memory element to a digital count value using a digital counter.

5. The method of claim 4, wherein the count in the digital counter represents the difference between the known and unknown states of the memory element.

6. The method of claim 4, wherein the digital counter has a reversible direction.

7. The method of claim 1, wherein buffering is accomplished using registers.

8. The method of claim 7, wherein the registers include synchronous dynamic random access memory.

9. A method for reducing read time of memory values in magnetic memory array, comprising:

(a) sampling an unknown state of a first memory element;

(b) buffering this sampled value;

(c) repeating (a) and (b) for subsequent memory elements;

(d) writing a known value to the first memory element;

(e) repeating (d) for the subsequent memory elements;

(f) sampling the known value written to the memory elements;

(g) comparing the buffered value with the known value; and

10. The method of claim 9, wherein sampling the memory element includes:

regulating a voltage across a memory element; and

correlating the resistance of a memory element to a digital count value using a digital counter;

wherein the memory element comprises a magnetic memory element.

11. The method of claim 10, wherein the count in the digital counter represents the difference between the known and unknown states of the memory element.

12. The method of claim 11, wherein the digital counter is an up/down counter.

13. The method of claim 9, further comprising restoring the original unknown state to the memory elements

14. A memory, comprising:

a plurality of magnetic memory elements;

a sense element coupled to the memory elements;

a digital counter coupled to the sense element, wherein the count contained in the counter is related to the digital value of a memory element; and

a plurality of registers coupled to the counter, wherein each register is configured to store a count value.

15. The memory of claim 14, further comprising an arithmetic logic unit for performing mathematical operations on the contents of the registers.

16. The memory of claim 14, wherein the counter contains the sum and difference of digital count values.

17. The memory of claim 14, wherein self-referencing techniques are employed to read the value of a memory element.

18. The memory of claim 14, wherein an unknown data value is represented by a first count of the digital counter, and this count is retained in the register.

19. The memory of claim 18, wherein a known data value is represented by a second count of the digital counter, and wherein the first and second counts are compared.

20. The memory of claim 19, wherein the second count is contained in a register and the comparison is performed using mathematical operations.

21. A method for reading memory values, comprising:

coupling a digital counter to a memory element;

associating a first digital count with an unknown data value contained in the memory element;

retaining the first digital count;

associating a second digital count with a known value contained in the memory element; and

comparing the first and second digital counts.

22. The method of claim 21, wherein the first and second digital counts are retained in a register that is coupled to the digital counter.

23. The method of claim 21, wherein the first digital count is contained in the digital counter and the direction of the digital counter is reversed prior to associating the second digital count with the known value.

24. A computer system, comprising:
a processor;
a keyboard coupled to the processor; and
a system memory coupled to the processor, wherein the memory comprises:
an array of memory elements;
sensing circuitry coupled to the memory elements;
counter circuitry coupled to the sensing circuitry, wherein the counter contains a count indicative of the digital value of a memory element; and
a plurality of registers coupled to the counter capable of storing multiple count values.

25. The computer of claim 24, wherein the memory further comprises an arithmetic logic unit to perform mathematical operations on the contents of the registers.

26. A memory, comprising:
storage means for storing information;
sensing means for sensing the stored information;
counting means wherein the count in said counting means is related to the digital value of the stored information; and
storage means for wherein the storage means is configured to store a count value.